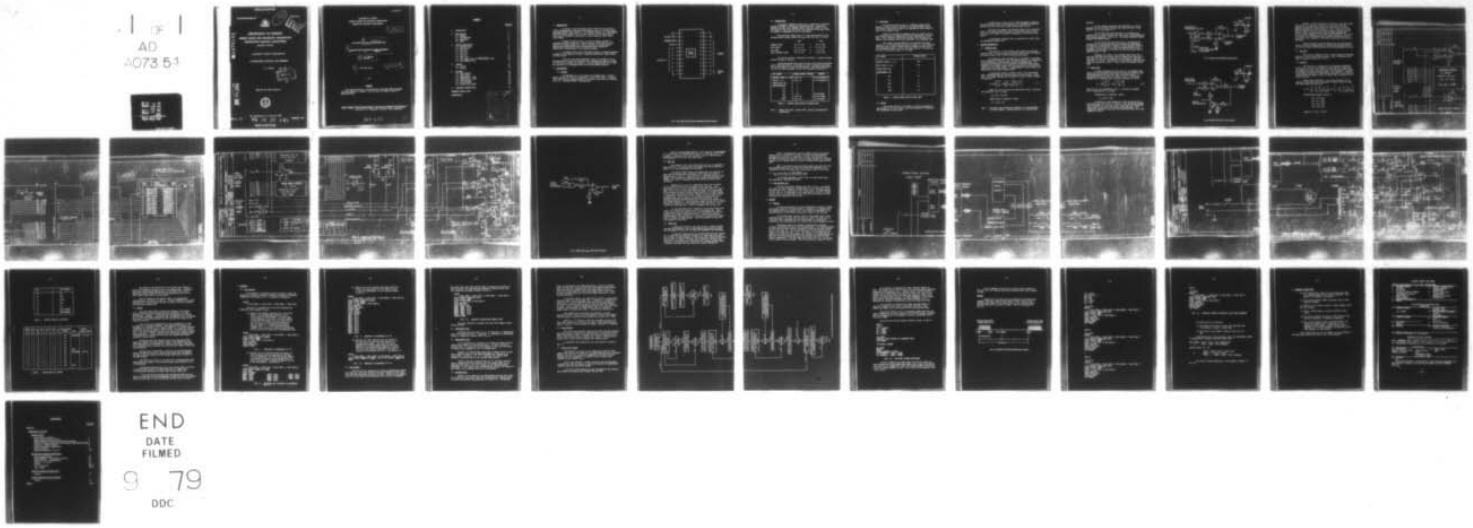
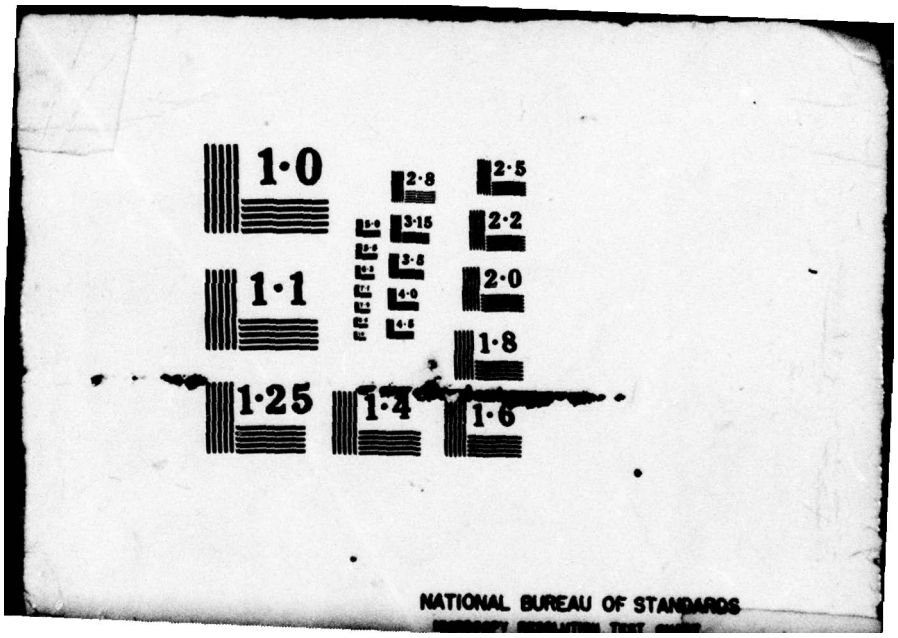
AD-A073 154 AERONAUTICAL RESEARCH LABS MELBOURNE (AUSTRALIA) F/G 9/2
A MICROPROCESSOR CONTROLLED PROM PROGRAMMER.(U)
FEB 79 C W SUTTON
UNCLASSIFIED ARL/AERO-TM-313 NL

1 OF 1
AD
A073 54



END
DATE
FILMED
9 79
DDC


1·0
1·1
1·25
2·8
3·15
3·5
4·0
4·5
1·4
2·5
2·2
2·0
1·8
1·6
NATIONAL BUREAU OF STANDARDS

ARL-AERO-TECH-MEMO-313

AR-001-602

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

AERONAUTICAL RESEARCH LABORATORIES

MELBOURNE, VICTORIA

Aerodynamics Technical Memorandum 313

A MICROPROCESSOR CONTROLLED PROM PROGRAMMER

C.W. SUTTON

COPY No 15

79 08 27 081

FEBRUARY, 1979

AR-001-602

DEPARTMENT OF DEFENCE

DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

AERONAUTICAL RESEARCH LABORATORIES

(12) 46 p.

(9) Aerodynamics Technical ~~Memorandum 313~~ memo

(6) A MICROPROCESSOR CONTROLLED PROM PROGRAMMER

(10) C.W. SUTTON

(14) ARL/AERO-TM-313

(11) Feb 79

—A—

SUMMARY

This paper describes a microprocessor controlled PROM Programmer with user options to program, list and copy the memory content of MM5204Q devices.

POSTAL ADDRESS: Chief Superintendent, Aeronautical Research Laboratories, Box 4331, P.O., Melbourne, Victoria, 3001, Australia.

CONTENTS

1. INTRODUCTION

A circuit, with associated control software for use with a "PACE" microprocessor (National Semiconductor Corp) is described which programmes MM5204Q Type memories. The MM5204Q package is a Programmable Read Only Memory (PROM) with a storage capacity of 512 words each of 8 bits and is erasable by exposure to a high intensity ultra violet light source.

Storage is non-volitile, in that the memory content is unchanged by power switch-off. Being reusable, the devices are very useful for reliable storage of control programs in microprocessor applications particularly where requirements could change and necessitate a modification to the control program.

To program (write into) the PROM requires a switching sequence of positive and negative voltage of specified amplitudes, pulse widths and duty cycles.

Control of the PROM programmer circuit is through a 16 bit microprocessor in which the software also automatically checks the PROM for errors and provides the option to list the PROM content and to copy the contents of a programmed PROM into another MM5204Q package.

2. PROM DETAILS

2.1 Package

The MM5204Q is a 24 pin quartz lid package (Fig. 1) with a memory capacity of 4096 bits arranged as 512 by 8 bit words. Positive true logic notation applies except for the data lines which are negative true (i.e. inverted) during a program made.

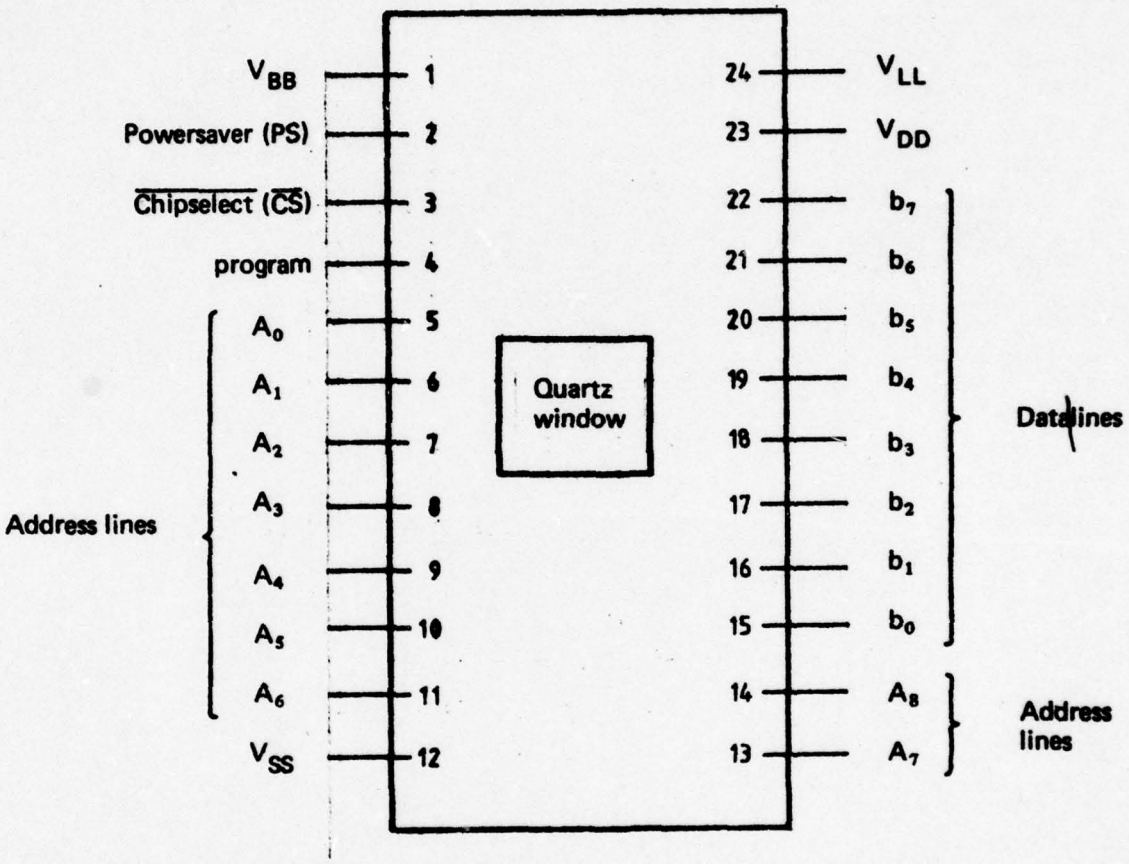


FIG. 1. PIN IDENTIFICATION OF MM5204Q PROM PACKAGE

2.2 Program Mode

To program a MM5204Q requires that a sequence of specified voltage waveforms be applied to the PROM package. During the sequence the V_{BB}, V_{DD} & PROGRAM (PROG) lines are pulsed to store the states of the 8 bit data word, then existing on the data lines, as charges in addressable cells of the memory.

The specified ranges (Ref. 1) in the program mode for the switched input voltage levels with $V_{SS} = \overline{CS} = PS = V_{LL} = 0$ volts

	HIGH		LOW
ADDRESS LINES:	+0.3 to -2V	&	-11 to -50V
DATA LINES:	+0.3 to -2V	&	-11 to -18V
V_{BB} LINE:	11.4 to 12.6V	&	0 to +4V
V_{DD} & PROGRAM LINES:	+0.5 to -2V	&	-48 to -50V

The switch circuits, described in Section 3, produce voltage levels as shown in Table 1.

Specified maximum duty cycle for V_{DD} is 25% with the program pulse width specified to be between 0.5 and 5 milliseconds and V_{DD} set-up time between 40 and 100 microseconds. The pulse characteristics of the PROM programmer circuit are discussed in Section 4.

PIN INDENT.	VOLTAGE LEVELS (VOLTS)	CURRENT
ADDRESS LINES A_0 - A_8	0 and -14	10 milliamps/bit
DATA b_0 - b_7	0 and -14	10 milliamps/bit
POWER SAVER (PS)	0	-
$\overline{\text{CHIP SELECT}}$ (CS)	0	-
V_{SS}	0	-
V_{LL}	0	-
V_{BB}	+12	50 milliamps
V_{DD}	0 and -48	200 milliamps
PROG	0 and -48	10 milliamps

TABLE 1. VOLTAGE LEVELS USED TO PROGRAM PROM.

REF. 1. Memory Data Book, January 1976, National Semiconductor Corporation.

2.3 Read Mode

To read the stored content of a MM5204Q requires that specific voltage levels be applied to the PROM package and for the states of the 8 data lines to be recorded for each change of state of the address lines.

Except for the data and address lines all other lines to the PROM are held at predetermined voltages throughout the read mode. These voltages, except for pins V_{LL}, $\overline{CS}$ & PS which are earthed, are different from those required in the programme mode.

The voltage levels produced by the switching circuits (Section 3) in the read mode are shown in Table 2. The Transistor Transistor Logic (TTL) voltages for the address and data lines are switchable between 0 to 0.8 volts for "Low" or "0" state and +3.5 to 5.3 volts for "High" or "1" state.

PIN INDENT.	VOLTAGE LEVELS
ADDRESS LINES A_0 - A_8	TTL
DATA LINES b_0 - b_7	TTL
POWER SAVER (PS)	0
CHIP SELECT ($\overline{CS}$)	0
V_{SS}	+5
V_{LL}	0
V_{BB}	+5
V_{DD}	-12
PROG	+5

TABLE 2. VOLTAGE LEVELS USED TO READ PROM.

2.4 Erase

The stored content of the PROM is erased by exposure of the package to an ultra violet light source placed to illuminate the transparant quartz window.

A sliding tray, built into the PROM programmer, positions the PROM package within 15 millimetres of an enclosed horizontally mounted 240 volt ultra violet lamp (Philips Type TUV 6W).

With this arrangement the charges stored in the individual cells of the memory chip are allowed to decay such that all data bits read "Low" within 10 minutes of exposure to the ultra violet source.

A satisfactory exposure time is therefore ½ an hour using an overexposure factor of 2.

3. CIRCUIT DESCRIPTION

3.1 Address Lines

From Tables 1 & 2 the address lines need to be switched between 0 and -14 volts during the program (write) mode and between TTL levels (say 0 and +4 volts) during the read mode.

The change in level and polarity is conveniently provided by an operational amplifier with TTL signals applied, as appropriate, to the inverting or non-inverting inputs of the amplifier. By arranging the amplifier to have fixed but different voltage gains, referred to the common output, for the inverting and non-inverting inputs then the output signal is predetermined in both polarity and amplitude for TTL input voltage levels.

A simplified circuit is shown in Fig. 2 for one address line. Waveforms show the voltage levels and logic states. From REF. 2 the output voltage (E) is related to the two input voltages E1 and E2 by:

$$E = -E1\left[\frac{R2}{R1}\right] + E2\left[\frac{R4}{R3 + R4}\right]\left[\frac{R1 + R2}{R1}\right] \qquad (1)$$

Where R1, R2, R3 and R4 are identified in Fig. 2 and have the values R1 = R4 = 3 k ohm

R2 = R3 = 18 k ohm

Substituting in equation 1 gives

$$E = -6.E1 + E2$$

REF. 2. Evolution From Operational Amplifier To Data Amplifier, by Robert Demrow. Analogue Devices, Inc E010-40-9/68.

Consider:

(a) The standby case where both AND gates A1 & A2 are disabled, by the low logic states of the read and write lines, then E1 ≈ E2 ≈ 0 and hence E ≈ 0.

(b) The read case where AND gate A1 is disabled and therefore E1 ≈ 0 and E2 follows the logic state of the address bit from the microprocessor, then E ≈ E2. The output therefore swings between TTL voltage levels.

(c) The write case where AND gate A2 is disabled and therefore E2 ≈ 0 and E1 follows the TTL states of the address bit from the microprocessor. However, as the amplifier clips at an output level of about ±14 volts, the address lines are not subjected, in practice, to six times the TTL high level state as expected with E ≈ -6E1.

Although +0.8 volts is the accepted upper limit for a TTL logic low state the actual value is usually much less and -6 times the TTL low state voltage has been measured as typically less than -0.5 volts. From Section 2.2 the address lines for this state are permitted to reach -2 volts during the program (Write) mode.

3.2 Data Lines

A similar technique to that used for the address lines applies but with important differences because the address lines are unidirectional and the data lines are bidirectional. A simplified data line circuit is shown in Fig. 3. The output voltage (E) is related to the two input voltages E1 & E2 by

$$E = -E1\left[\frac{R2}{R1}\right] + E2\left[\frac{R1 + R2}{R1}\right] \qquad \ldots(2)$$

Where R1 & R2 are identified in Fig. 3, and have the values R1 = 3 k ohms and R2 = 13 k ohms.

Substituting in equation 2 gives:

$$E \approx -4.E1 + 5.E2$$

As before, in the standby case, both E1 and E2 are at low state logic level and E ≈ 0 volts. Also, during the program mode E2 remains at a low state logic level while E1 follows the logic state of the data line from the microprocessor. The operational amplifier clips when the logic high value of E≈ -4E1 exceeds -14 volts.

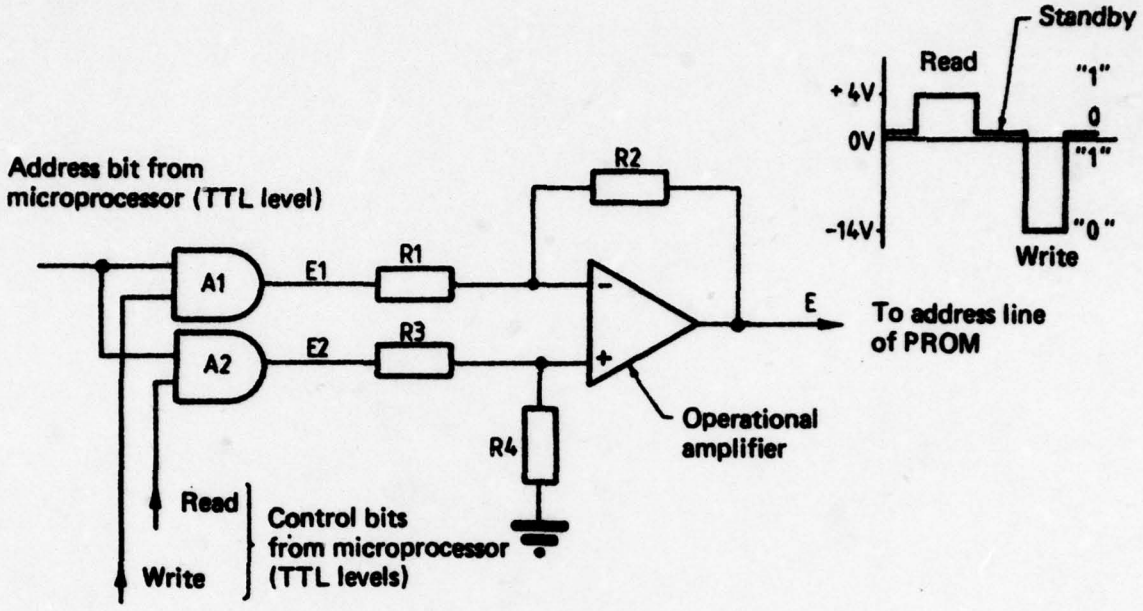


FIG. 2. SIMPLIFIED ADDRESS LINE CIRCUIT

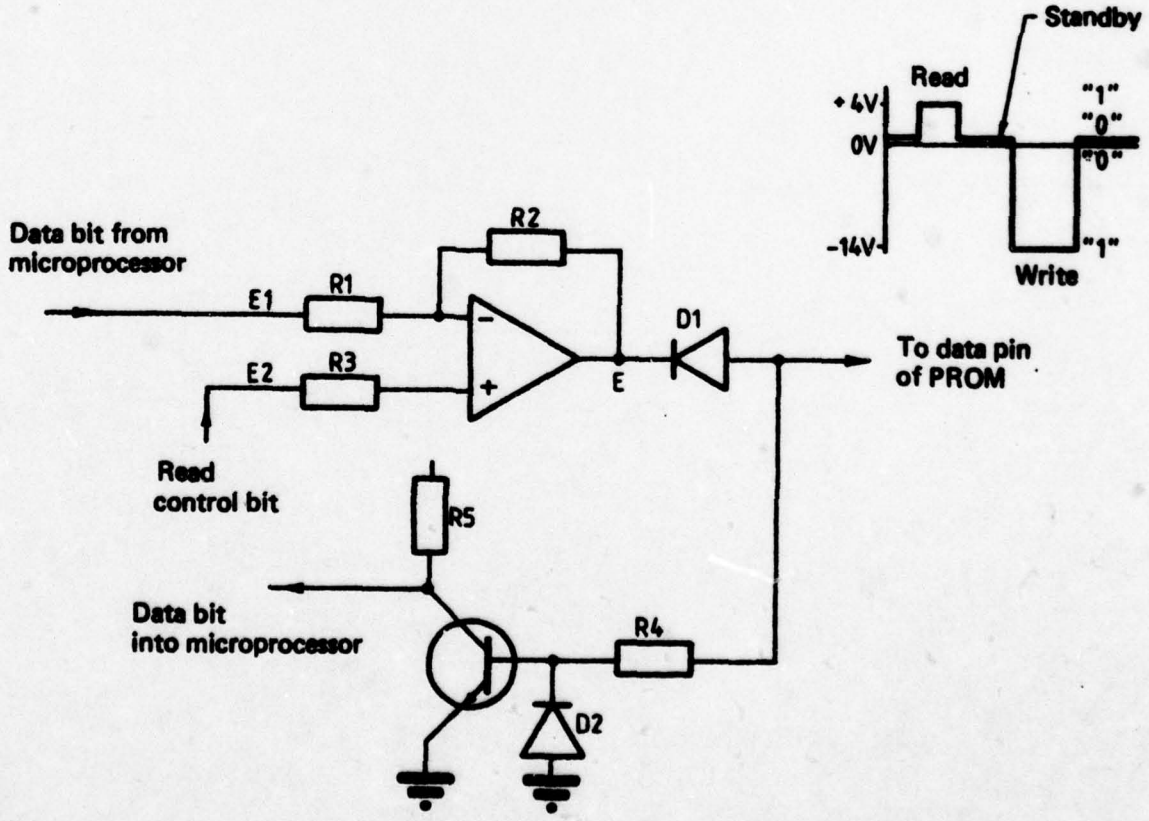


FIG. 3. SIMPLIFIED DATA LINE CIRCUIT

However, in the read mode E1 is held at a low state logic level while E2 is held at a high state logic level and the operational amplifier output limits at the level of +14 volts without reaching the value given by E = 5.E2. Thus in the read mode the diode D1 (Fig. 3) is reverse biased to isolate the TTL levels of data bits, originating from the PROM package, from the low output impedance of the operational amplifier. The invert of the data bit, originating from the PROM, is read during the read mode at the collector of the buffer transistor by the microprocessor.

Diode D2 remains reverse biased during the read mode but conducts during the program mode to protect the transistor from the -14 volt levels that then exist on the bidirectional data line.

3.3 V_{SS} Line

This line is required to be at 0 volts during the program mode and +5 volts during the read mode. This is achieved with a simple transistor switch Q13 in Fig. 4.

3.4 V_{BB} Line

The V_{BB} line is controlled by an operational amplifier circuit (Fig. 5) which is similar to those used for controlling the address and data lines except that two TTL level input signals are summed at the non-inverting input of the amplifier. Because of the impracticability of simultaneous operation in both read and program modes the summing action is always with E1 and/or E2 at a logic low state.

Hence, again from REF. 2, the output voltage E of the operational amplifier may be expressed in terms of the two input TTL level signals E1 and E2 as:

$$E = E1 \left[1 + \frac{R2}{R1}\right]\left[\frac{R3}{R3 + R4}\right] + E2 \left[1 + \frac{R2}{R1}\right]\left[\frac{R4}{R3 + R4}\right]$$

Substituting resistor values of

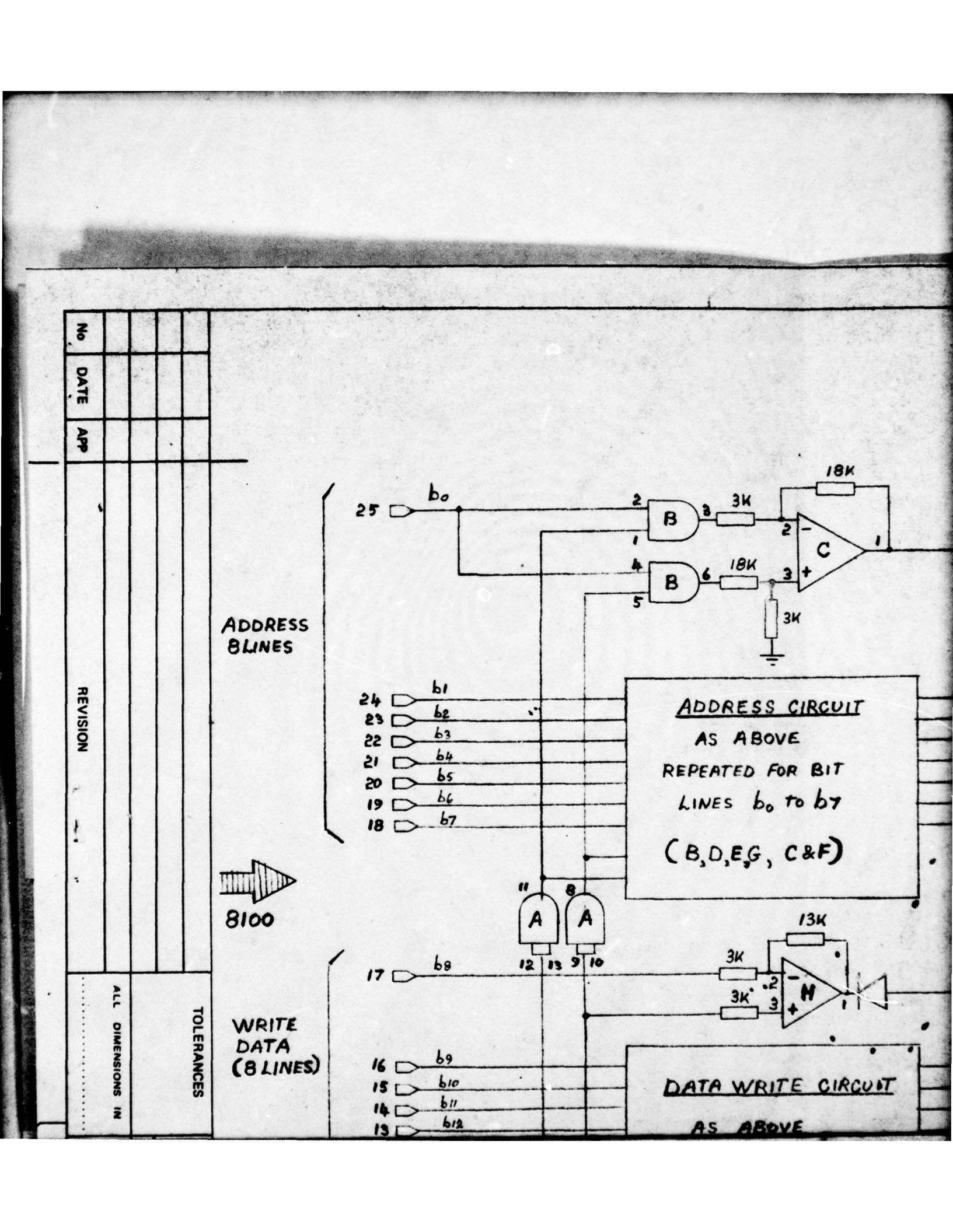
R1 = 3.9 k ohm

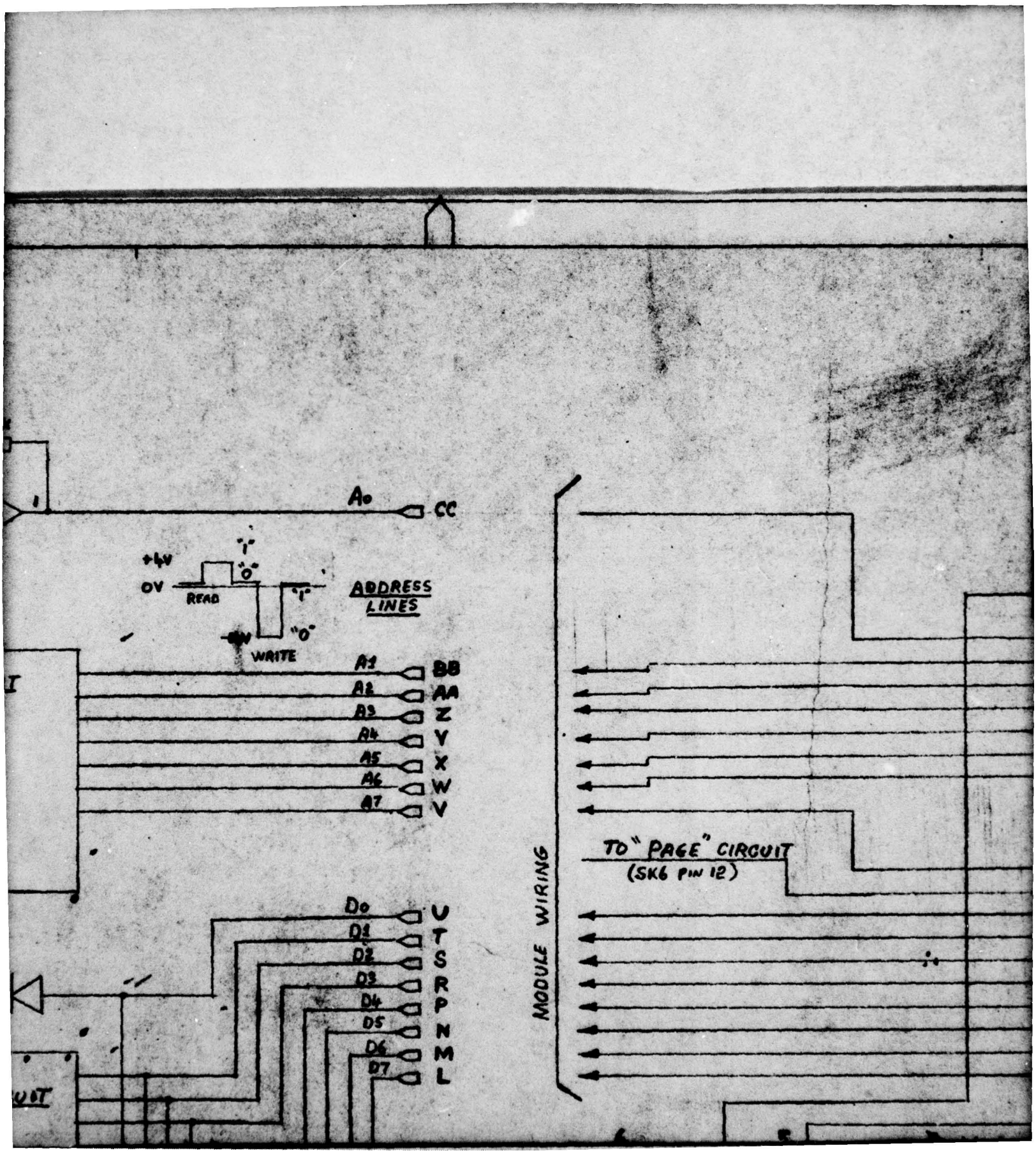
R2 = 13 k ohm

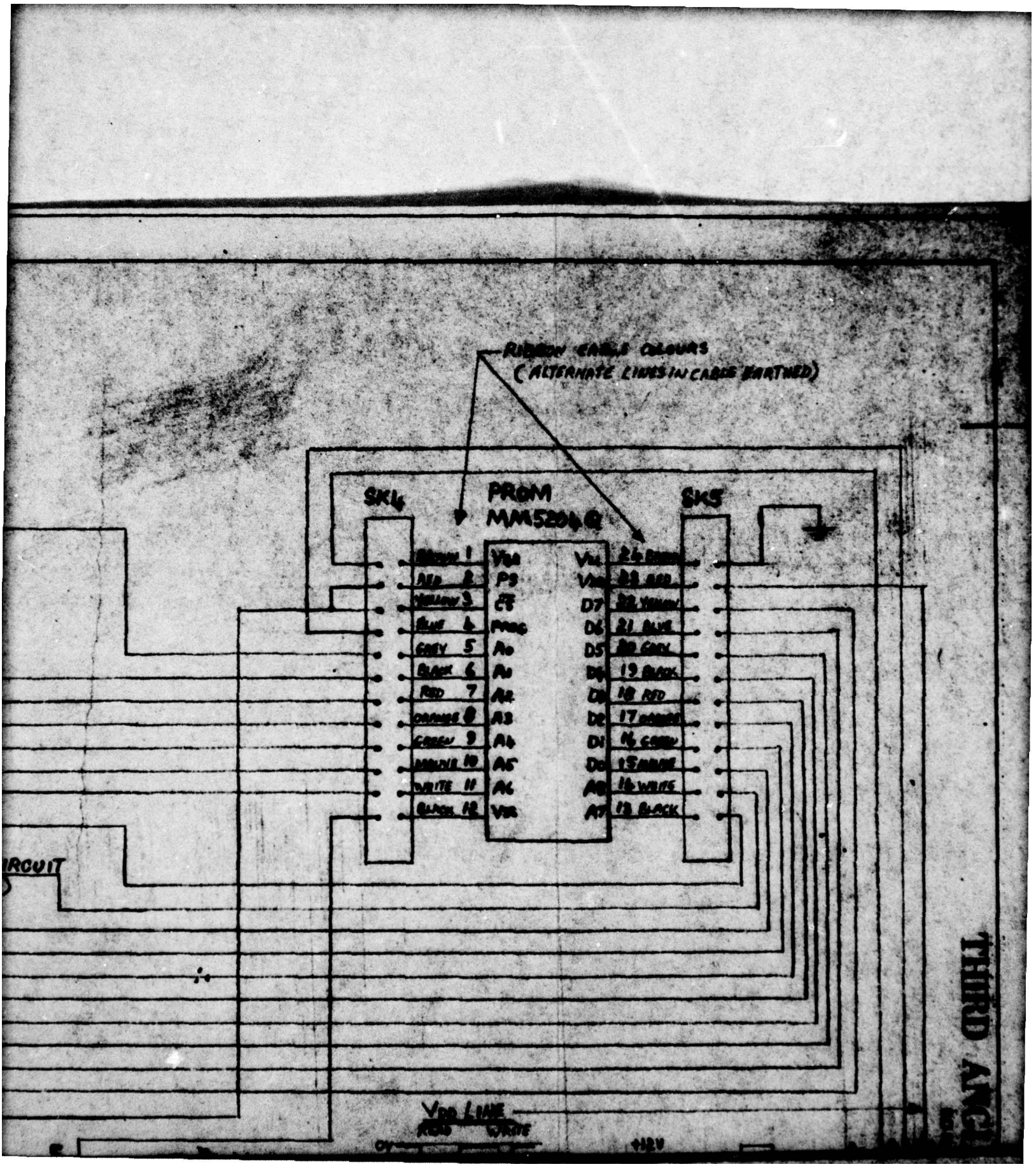
R3 = 2.2 k ohm

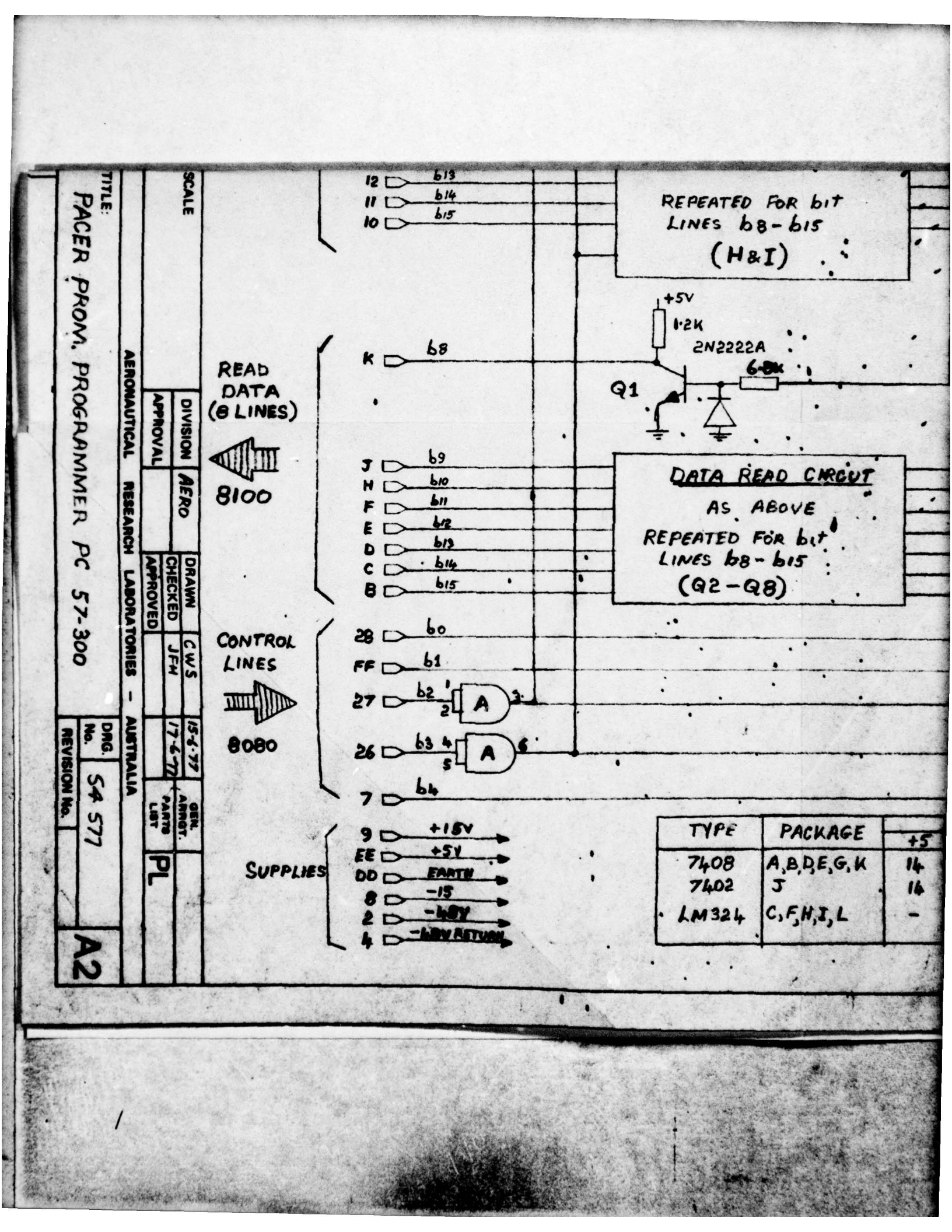
R4 = 6.8 k ohm

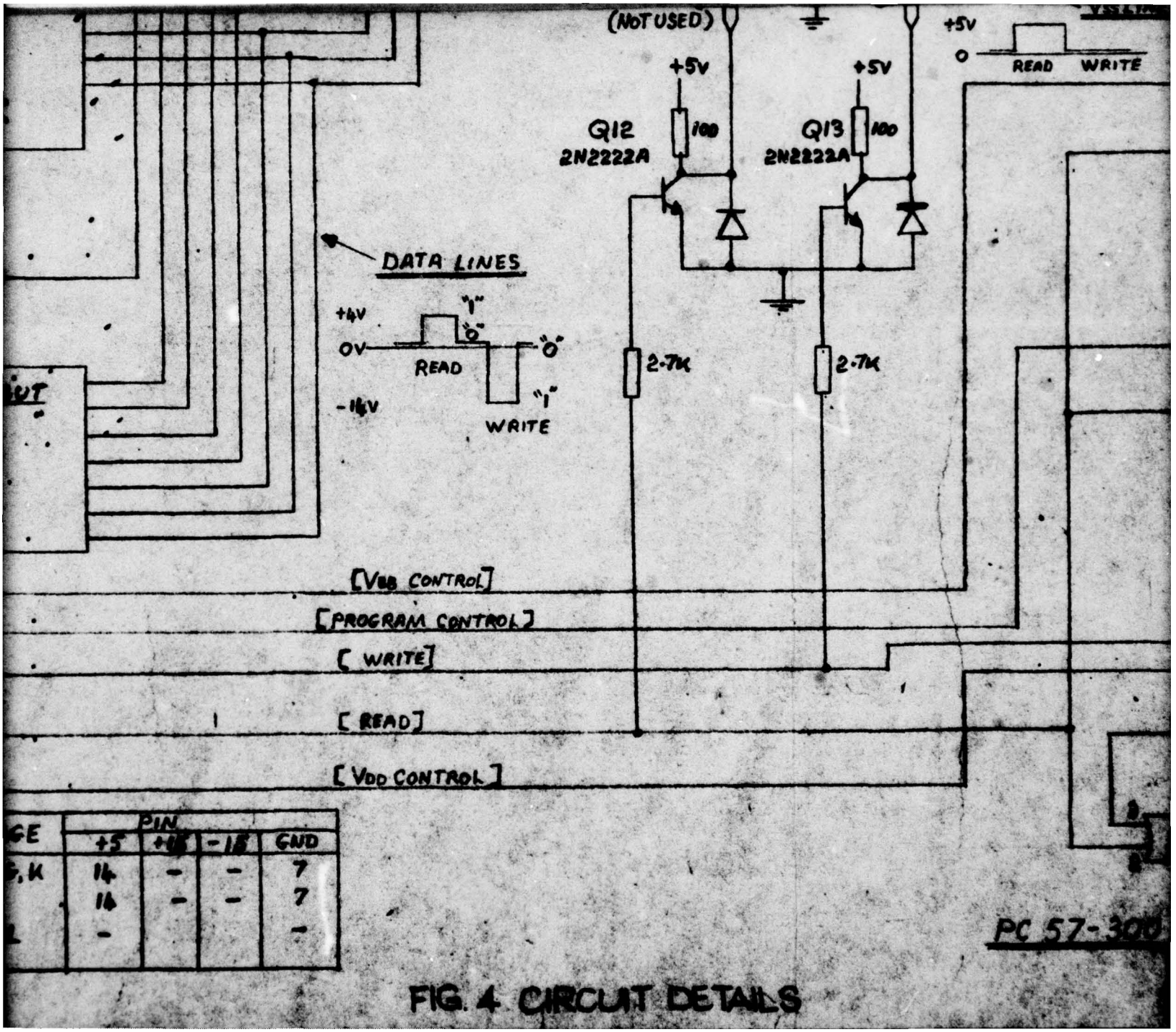
gives E = 1.1.E1 + 3.4.E2


No
DATE
APP
REVISION
ALL DIMENSIONS IN
TOLERANCES
ADDRESS 8 LINES
8100
WRITE DATA (8 LINES)
25 b0
24 b1
23 b2
22 b3
21 b4
20 b5
19 b6
18 b7
17 b8
16 b9
15 b10
14 b11
13 b12
B
B
C
A
A
H
18K
3K
18K
3K
13K
3K
3K
ADDRESS CIRCUIT
AS ABOVE
REPEATED FOR BIT
LINES b0 to b7
(B, D, E, G, C&F)
DATA WRITE CIRCUIT
AS ABOVE


A0
CC
+4V
0V
"1"
"0"
READ
"1"
-4V
"0"
WRITE
ADDRESS LINES
A1
A2
A3
A4
A5
A6
A7
BB
AA
Z
Y
X
W
V
D0
D1
D2
D3
D4
D5
D6
D7
U
T
S
R
P
N
M
L
MODULE WIRING
TO "PAGE" CIRCUIT
(SK6 PIN 12)

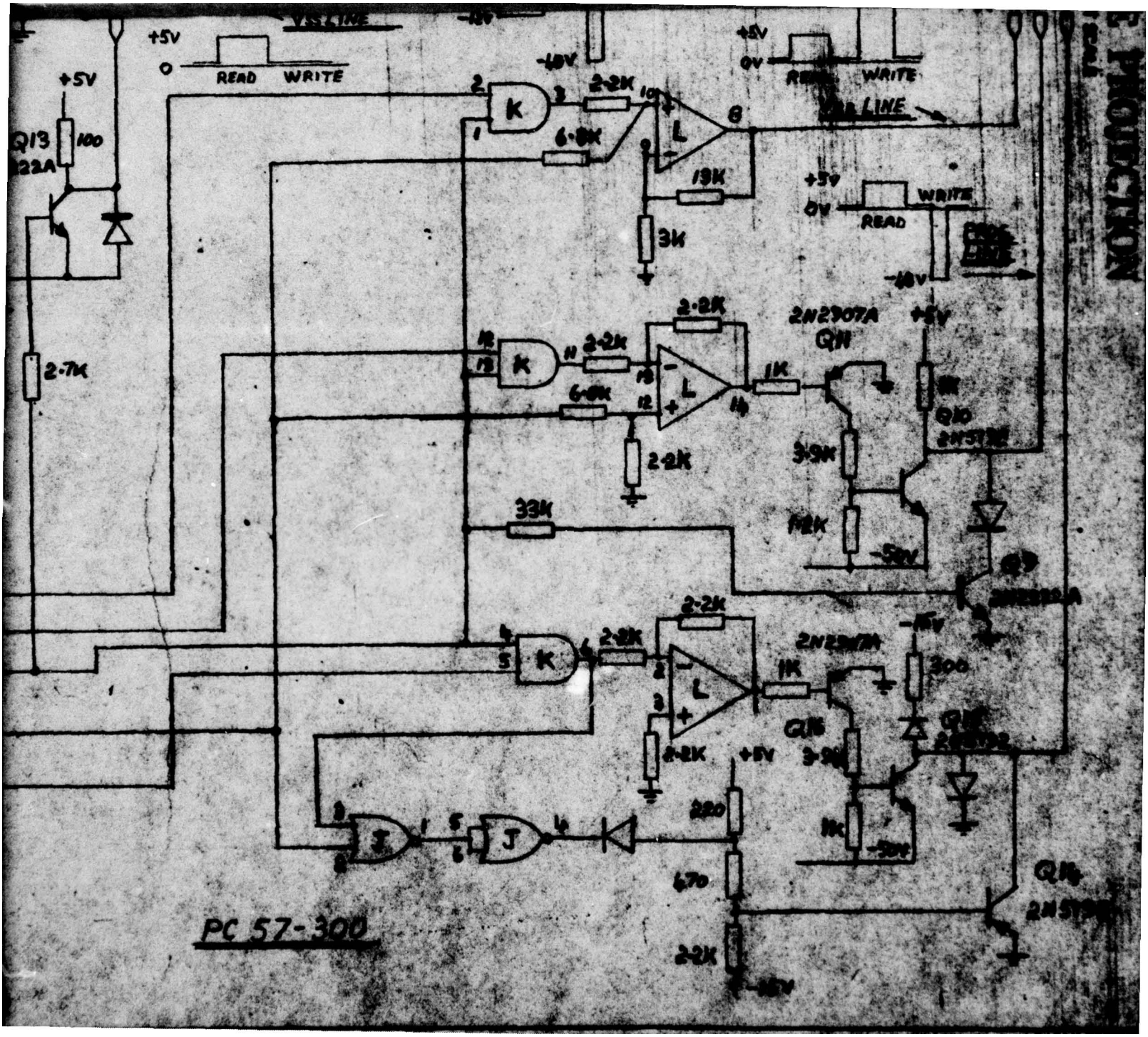

RIBBON CABLE COLOURS
(ALTERNATE LINES IN CABLE EARTHED)
SK4
PROM
MM5204Q
SK5
BROWN 1
RED 2
YELLOW 3
BLUE 4
GREY 5
BLACK 6
RED 7
ORANGE 8
GREEN 9
BROWN 10
WHITE 11
BLACK 12
Vss
P3
CE
PROG
A0
A1
A2
A3
A4
A5
A6
Vbb
Vcc
D7
D6
D5
D4
D3
D2
D1
D0
A8
A7
24 BROWN
23 RED
22 YELLOW
21 BLUE
20 GREY
19 BLACK
18 RED
17 ORANGE
16 GREEN
15 BROWN
14 WHITE
13 BLACK
IRCUIT
VDD LINE
READ
WRITE
0V
+12V
THIRD ANG


TITLE:
PACER PROM PROGRAMMER PC 57-300
AERONAUTICAL RESEARCH LABORATORIES - AUSTRALIA
SCALE
DIVISION AERO
APPROVAL
DRAWN GWS
CHECKED JFH
APPROVED
15-4-77
17-6-77
GEN. ARRGT.
PARTS LIST PL
DRG. No. 54 577
REVISION No.
A2
READ DATA (8 LINES)
8100
CONTROL LINES
8080
SUPPLIES
12 b13
11 b14
10 b15
REPEATED FOR bit LINES b8-b15 (H&I)
+5V
1·2K
2N2222A
6·8K
Q1
K b8
J b9
H b10
F b11
E b12
D b13
C b14
B b15
DATA READ CIRCUIT
AS ABOVE
REPEATED FOR bit LINES b8-b15 (Q2-Q8)
28 b0
FF b1
27 b2
26 b3
7 b4
A
9 +15V
EE +5V
DD EARTH
8 -15
2 -48V
4 -48V RETURN
TYPE
PACKAGE
+5
7408 A,B,D,E,G,K 14
7402 J 14
LM324 C,F,H,I,L -



GE	PIN			
	+5	+12	-12	GND
5,4	14	-	-	7
	14	-	-	7
L	-			-

FIG. 4 CIRCUIT DETAILS


+5V
READ
WRITE
-10V
2·2K
6·8K
19K
3K
Q13
2N2222A
100
2·7K
33K
2N2907A
Q11
1K
3·9K
2·2K
Q10
2N3702
300
220
470
PC 57-300

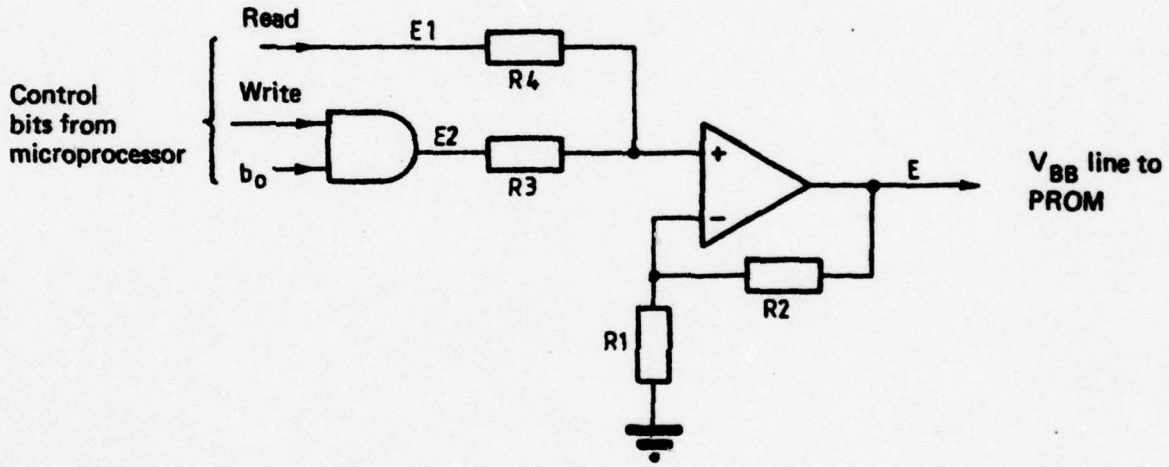


FIG. 5. SIMPLIFIED V_{BB} LINE DRIVE CIRCUIT

Thus in the read mode when E2 ≈ 0 the V_{BB} line is approximately +5 volts and in the program mode when E1 ≈ 0 the V_{BB} line is able to switch to nominally +12 volts provided control bit b0 from the microprocessor is at a TTL logic high level.

3.5 V_{DD} Line

From Tables 1 and 2 the voltage level of V_{DD} is required to pulse from 0 to -50 volts during the program mode and to maintain a level of -12 volts throughout the read mode.

At specific times during the program mode, the control bit (b4) from the microprocessor produces a TTL logic high level at package K pin 6 (Fig. 4). This results in a negative voltage at the output of the operational amplifier which causes transistor Q16 to conduct and switch on transistor Q15 which pulls the V_{DD} line to -50 volts.

Whenever K pin 6 is at a high logic level Q14 is biased off to avoid a short circuit to ground on the V_{DD} line. The switching action of Q14 is controlled by the logic state of J pin 4. When J pin 4 is at a logic high level the diode, (D4), associated with the three resistor voltage divider network, is reverse biased. In this state the network connects between +5 and -15 volts and Q14 is biased off. When J pin 4 is at a logic low level diode D4 is forward biased and the network is effectively modified to two resistors connected between ground and -15 volts which results in Q14 becoming biased on. This condition clamps the V_{DD} line to ground during the remainder of the program mode cycle when K pin 6 is at a logic low level and the -5 volts is removed from the V_{DD} line.

In the read mode K pin 6 remains at a low logic level with J pin 4 at a high logic level to turn off transistor Q14. This allows the V_{DD} line to be pulled to -12 volts through the 300 ohm resistor and forward conducting diode D5. Diode D5 is reverse biased whenever the V_{DD} line is at -50 volts to ensure that current flow is through the PROM package. Diode D6 protects the V_{DD} line from positive transitions.

3.6 PROG Line

A simplified version of the V_{DD} circuit is used to switch the PROG line between 0 and -50 volts during the write mode cycle and to maintain +5 volts on the PROG line throughout the read mode.

At specific times during the program mode cycle the control bit b1 from the microprocessor changes to a logic high state and K pin 11 (Fig. 4) also changes to a logic high which causes transistors Q11 and Q10 to conduct. The PROG line switches to -50 volts and diode D3, in the collector of transistor Q9, becomes reverse biased to prevent the PROG line from shorting to ground through Q9.

After a predetermined time the software controlling program causes K pin 11 to switch to a logic low level and thus bias-off transistors Q10 and Q11 to remove the -50 volt from the PROG line. The PROG line would be pulled to the +5V supply, through the collector resistor of Q10, except that Q9 is able to conduct and clamp the PROG line.

When a read mode occurs the write control line (bit b2) from the microprocessor goes to a logic low state and transistor Q9 is turned-off to allow the PROG line to be pulled to the +5 volt level.

3.7 $\overline{V_{LL}}$, Power Saver and $\overline{\text{Chip Select}}$ Lines

In the PROM programmer circuit (Fig. 4) these three lines are permanently connected to ground.

3.8 Page Address Line

The most significant address line (A8) in Fig. 1 is treated as a page line which enables the PROM memory to be considered as two sections each with a capacity of 256 X 8 bit words. The page address circuit (Fig. 6) is identical to that described in Section 3.1 except that the A8 line is controlled by the state of bits b5 and b6 of the microprocessor generated control word.

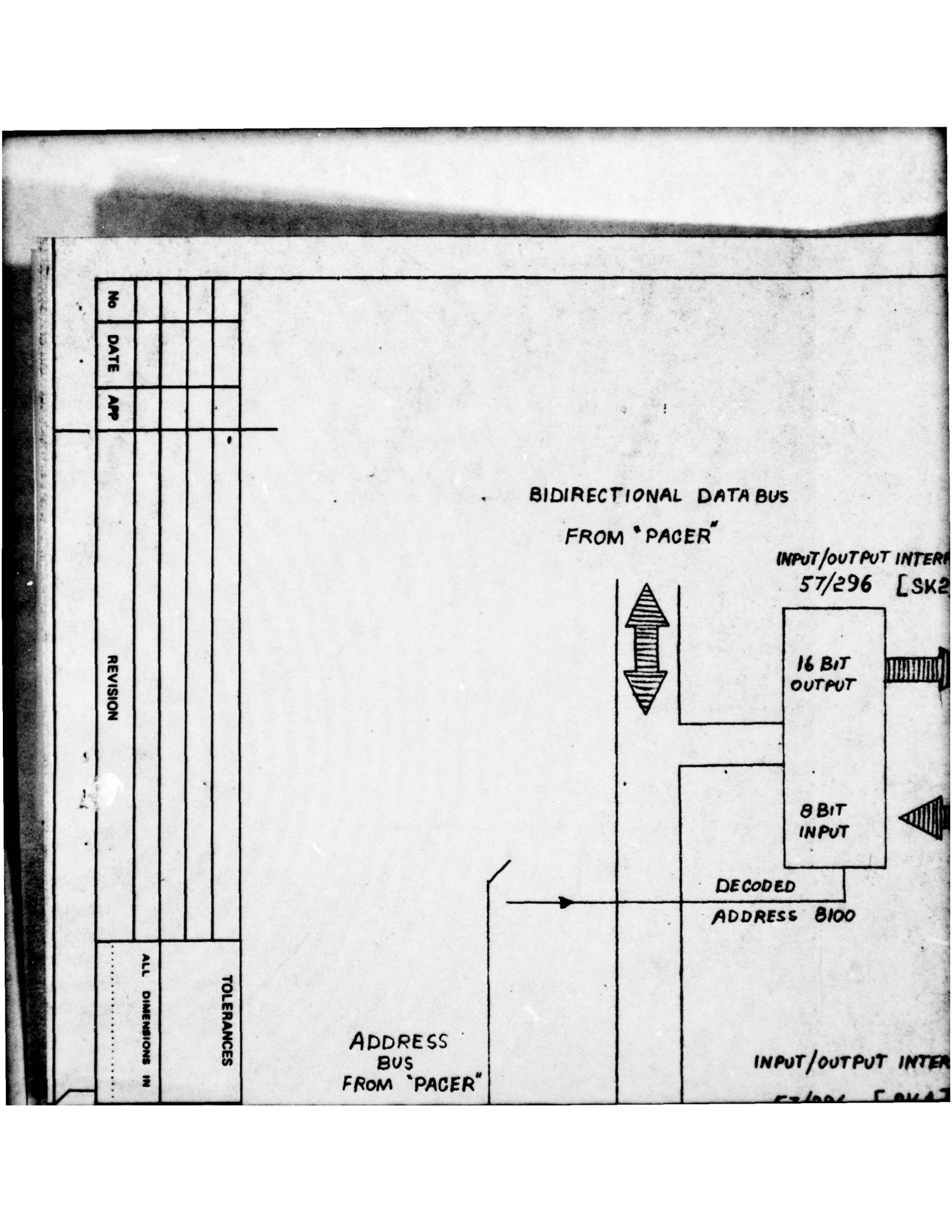
4. CONTROL

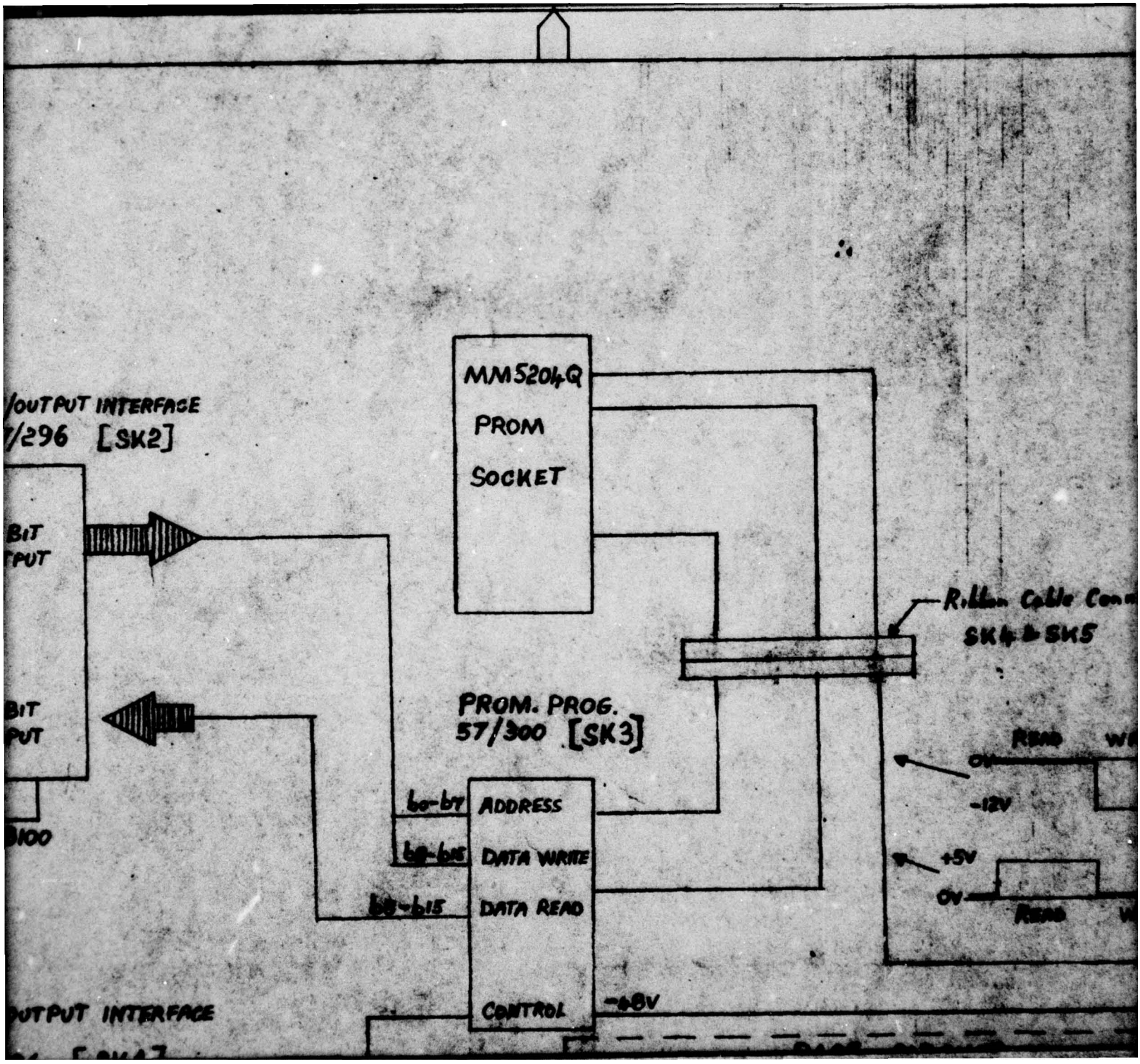
4.1 General

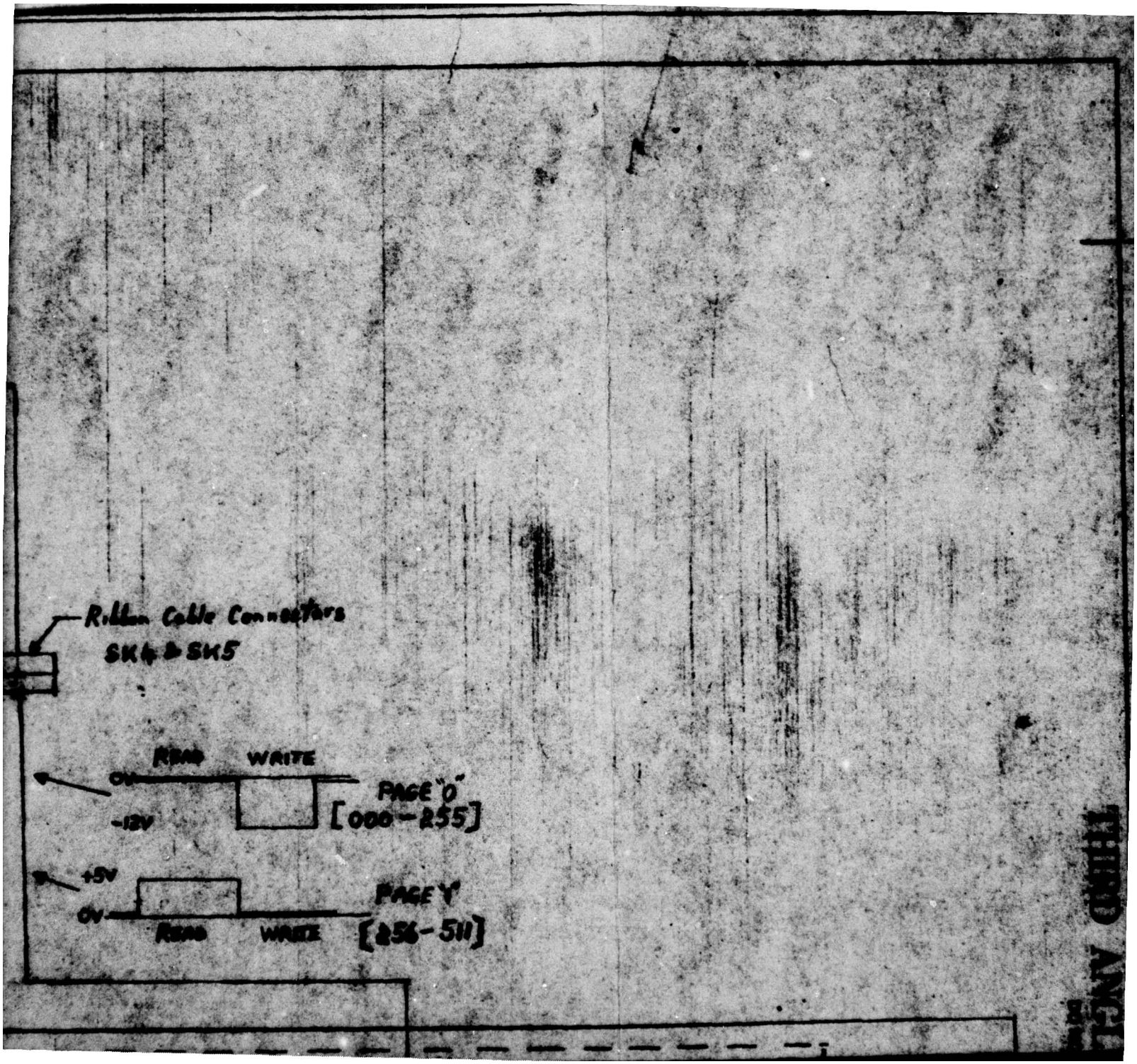
In the program mode the circuits described in Section 3 change the voltage levels to the PROM package in response to a combined data and address word and a control word. Both words are generated by the microprocessor and individually latched as inputs to the circuits.

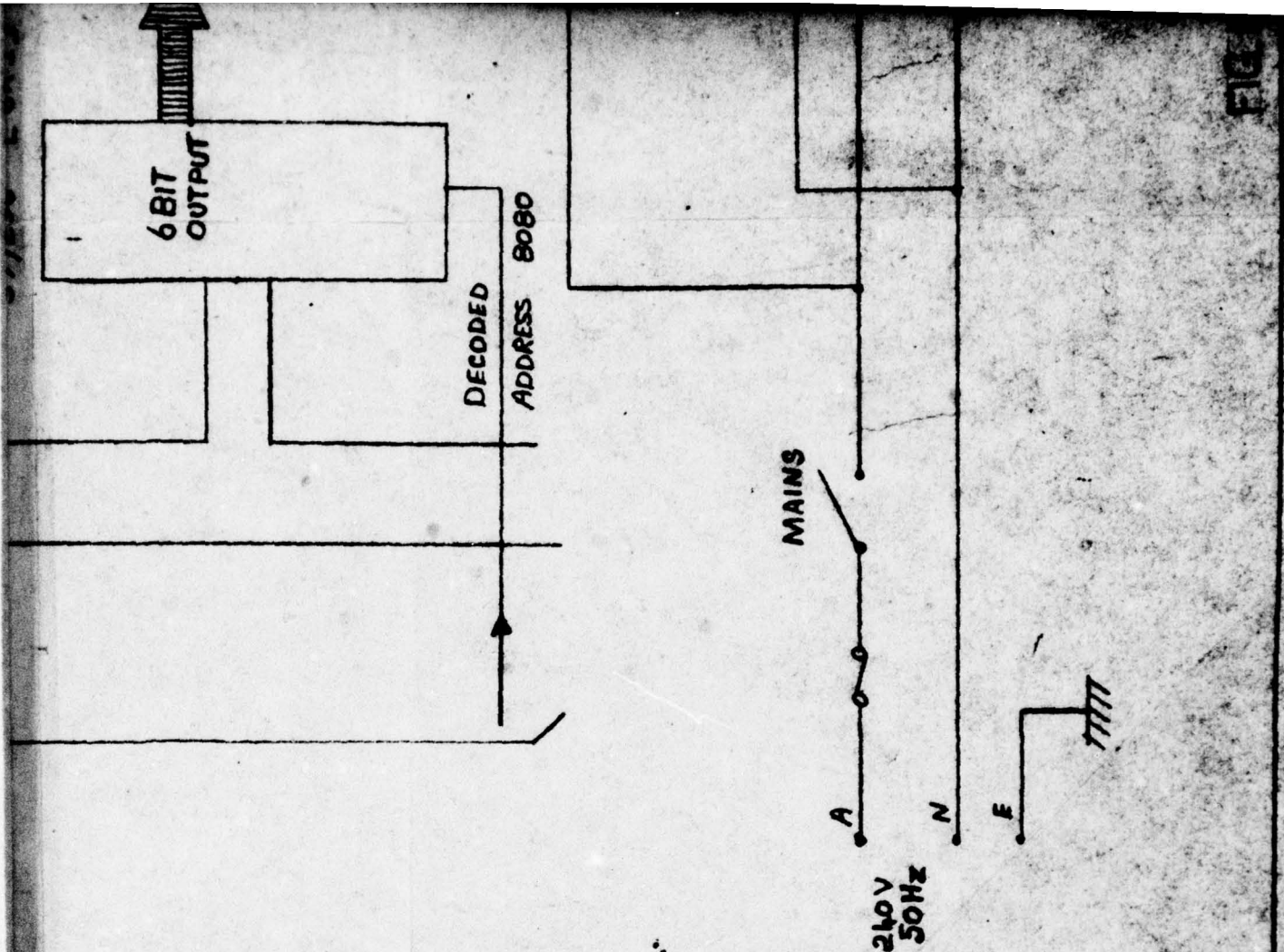
In the read mode a similar action occurs except that in the combined word all the data bits are held to a logic low level and the 8 bit data word, addressed from the PROM package, is latched and accepted by the microprocessor as an output from the programmer circuits.

The digital words are latched by input/output interface circuits associated with the 16 bit microprocessor. The combined address and data word provides address information (excluding the page address) in the lower byte (b_0 - b_7) and the data word, to be written into the PROM, in the upper byte (b_8 - b_{15}). The control word determines the sequence and timing of the voltage level changes to the PROM package for both the read and program modes and also provides the required page address information. Only the seven lower order bits (b_0 - b_6) of the 16 bit control word are needed. The bit allocation is shown in Table 3.


No
DATE
APP
REVISION
ALL DIMENSIONS IN
TOLERANCES
BIDIRECTIONAL DATA BUS
FROM "PACER"
INPUT/OUTPUT INTERF
57/296 [SK2
16 BIT
OUTPUT
8 BIT
INPUT
DECODED
ADDRESS 8100
ADDRESS
BUS
FROM "PACER"
INPUT/OUTPUT INTER


MM5204Q
PROM
SOCKET
/OUTPUT INTERFACE
7/296 [SK2]
BIT
TPUT
BIT
PUT
PROM. PROG.
57/300 [SK3]
b0-b7
ADDRESS
b8-b15
DATA WRITE
b8-b15
DATA READ
CONTROL
-48V
OUTPUT INTERFACE
0V
-12V
+5V
0V


Ribbon Cable Connectors
SK4 & SK5
READ
WRITE
0V
-12V
PAGE "0"
[000-255]
+5V
0V
PAGE "1"
[256-511]
READ
WRITE



SCALE	DIVISION	AERO	DRAWN	CWS	16-6-77	GEN. ARRGT.	
	APPROVAL		CHECKED	JFH	20-6-77	PARTS LIST	PL
			APPROVED	[illegible]	[illegible]		

AERONAUTICAL RESEARCH LABORATORIES – AUSTRALIA

TITLE:
PACER-PROM INTERFACE DETAIL

DRG. No. 54 575 A2

REVISION No.

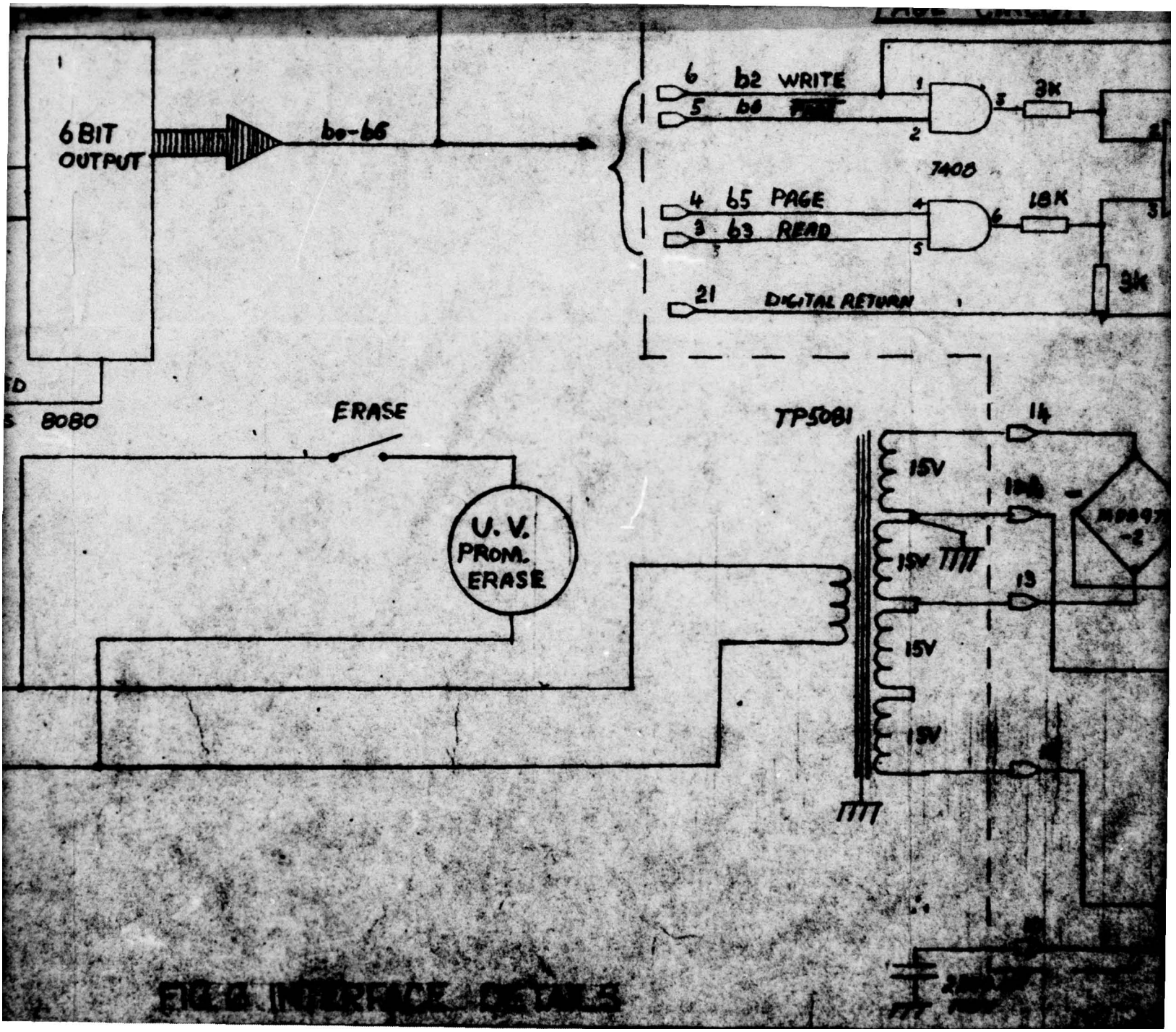
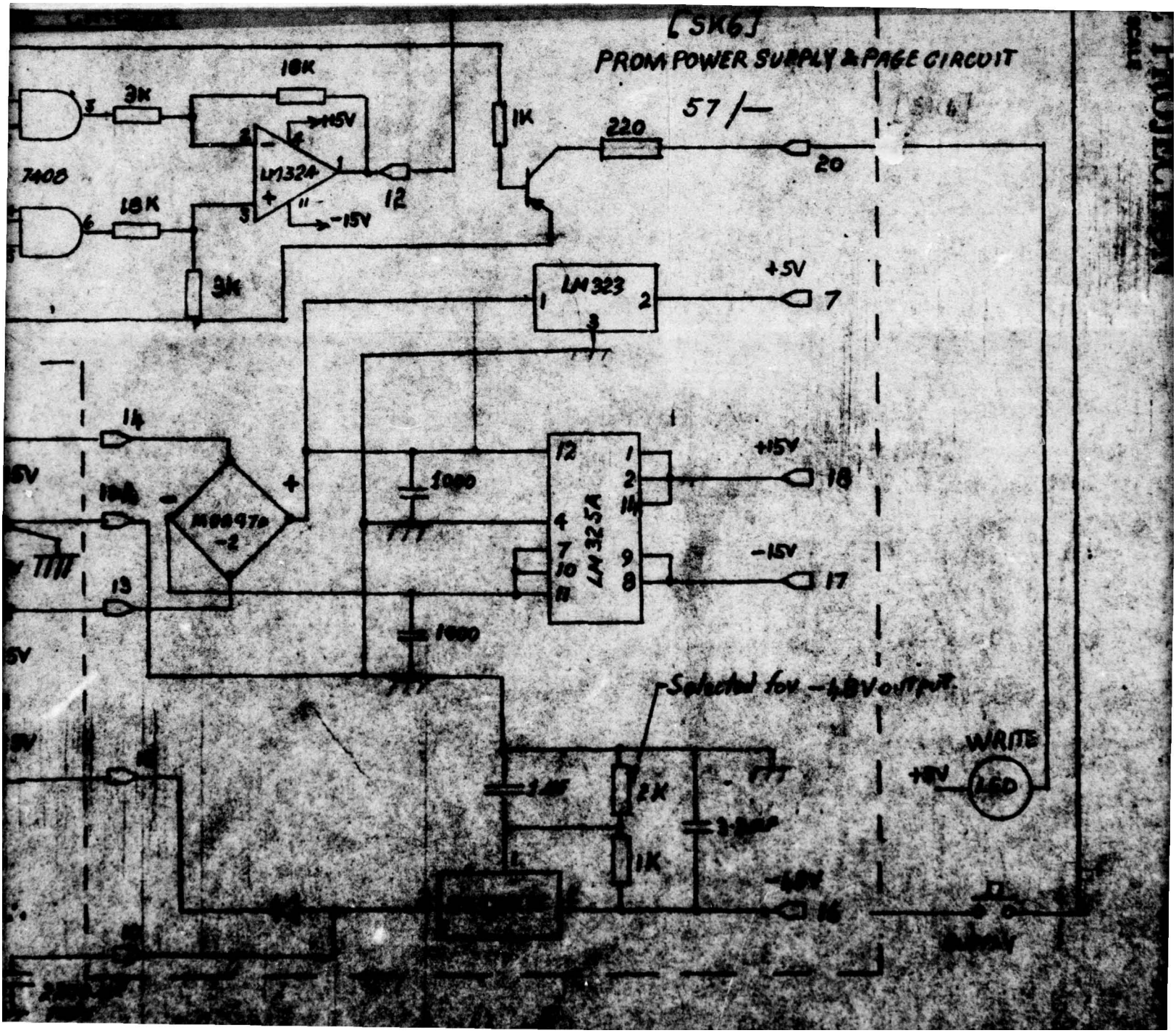


FIG 8 INTERFACE DETAILS


[SK6]
PROM POWER SUPPLY & PAGE CIRCUIT
57/—
3K
18K
+15V
LM1324
-15V
12
7400
18K
3K
1K
220
20
LM323
+5V
7
14
+15V
18
1000
LM325A
-15V
17
13
1000
Selected for -4.8V output.
WRITE
+5V
LED
2K
1K
-4.8V
16

BIT	LINE CONTROL
b_0	V_{BB}
b_1	PROG
b_2	WRITE
b_3	READ
b_4	V_{DD}
b_5	PAGE ADDRESS
b_6	$\overline{\text{PAGE ADDRESS}}$

TABLE 3. CONTROL WORD-BIT ALLOCATION.

$\overline{\text{PAGE}}$ b_6	PAGE b_5	V_{DD} b_4	READ b_3	WRITE b_2	PROG b_1	V_{BB} b_0	HEXADECIMAL NUMBER	MODE	MEMORY RANGE (PROM)
1	0	0	0	1	0	1	045	PROGRAMME	0 TO 255
1	0	1	0	1	0	1	055	"	" " "
1	0	1	0	1	1	1	057	"	" " "
1	0	1	0	1	0	1	055	"	" " "
1	0	0	0	1	0	1	045	"	" " "
1	0	0	1	0	0	0	048	READ	" " "
0	1	0	0	1	0	1	025	PROGRAMME	256-512
0	1	1	0	1	0	1	035	"	" "
0	1	1	0	1	1	1	037	"	" "
0	1	1	0	1	0	1	035	"	" "
0	1	0	0	1	0	1	025	"	" "
0	1	0	1	0	0	0	028	READ	" "

TABLE 4. CONTROL WORD BIT STATES.

The states of the seven bits of the control word change to switch the necessary voltage levels at the PROM package. Depending upon the selected memory address span of the PROM, five (or ten) sequential control words are used in the program mode and one (or two) control words used in the read mode.

The bit changes of the control words, with hexadecimal identification, are listed in Table 4. Voltage waveforms on the lines switched by the control words are shown in Figs. 4 and 6 for program and read modes respectively.

4.2 Timing

The time lapse between various bit changes in the control words is determined from the specification provided by the PROM manufacturer. However, in designing both the hardware and software for the PROM programmer, constraints were introduced by the instruction cycle time of the microprocessor and the rise and fall times of the switching circuits.

Only one of the microprocessor's four accumulators is able to output to a peripheral address. This requires that either the accumulator be reloaded, from a memory address, or a register exchange instruction be used to change a control word. To output the control word to the PROM programmer circuits also requires an indirect address store instruction. Either combination of instructions requires about 20 microseconds to perform and this sets the minimum time between sequential control words.

Because of the step response time of the Quad operational amplifiers (LM324) the rise and fall times of the address and data lines approximates 60 microseconds. However other lines, associated with transistor switch circuits, have rise and fall times of less than one microsecond.

The V_{DD} line is specified to switch 40 to 100 microseconds before the PROG line and it is during this period that the address and data lines are latched and the voltage levels able to settle at the PROM package.

The PROG line is held at -48 volts for 2.8 milliseconds which approximates the middle of the specified pulse width range of 0.5 to 5 milliseconds.

The maximum specified duty cycle for the V_{DD} pulse is 25% and a software delay allows the program mode cycle to repeat every 15 milliseconds resulting in a duty cycle of just under 20%.

In the read mode the minimum set-up times specified for the PROM are easily met by the microprocessor instruction time and adequate delays are provided to allow the address and data lines to settle.

5. SOFTWARE

5.1 User Options

The software is arranged to allow the user to input the necessary information through a keyboard in response to messages. Immediately the program is run it responds by displaying

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY
```

The user, in choosing one of the four possibilities determines the subsequent action.

(a) Typing P for program indicates that a data file held in the microprocessor memory is to be written into the PROM package. The start and finish addresses of the file, the start address of the PROM and whether the low or high byte of the file is to be stored are provided by the user in response to automatically generated messages (Fig. 7). In the following message examples those characters underlined were entered by the user and all values are in hexidecimal code.

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS ØØ29 END ØØ2E
PROM STARTS Ø1ØØ
BYTE; L FOR LOW, H FOR HIGH L
DATA ADDRESS
PROM PROM DATA
ERRORS ØØØØ
```

FIG. 7. MESSAGE IN RESPONSE TO "P"

(b) Typing L for list indicates that the content of the PROM memory range as specified by the user is to be displayed. The start and finish address is provided in response to the message (Fig. 8) which is followed by a heading and column listing of the PROM memory. See Section 5.3.

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY L
PROM STARTS Ø1ØØ END Ø1ØA
LIST PROM
DATA ADDRESS
ØØØD  Ø1ØØ          ØØØØ  Ø1Ø4          ØØØØ  Ø1Ø8
ØØ26  Ø1Ø1          ØØØØ  Ø1Ø5          ØØØØ  Ø1Ø9
ØØØA  Ø1Ø2          ØØØØ  Ø1Ø6          ØØØØ  Ø1ØA
ØØ26  Ø1Ø3          ØØØØ  Ø1Ø7
```

FIG. 8. MESSAGE AND LISTING IN RESPONSE TO "L"

(c) Typing B for both indicates that data words from a file are to be written into the PROM, (as for P) then the PROM memory is to be read and listed (as for L).

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY B
FILE STARTS ∅11∅ END ∅11A
PROM STARTS ∅11∅
BYTE; L FOR LOW, H FOR HIGH H
DATA ADDRESS
PROM PROM DATA
ERRORS ∅∅∅∅
LIST, PROM
DATA ADDRESS
∅∅A9  ∅11∅
∅∅F1  ∅111
∅∅19  ∅112
∅∅F1  ∅113
∅∅19  ∅114
∅∅18  ∅115
∅∅E5  ∅116
∅∅6A  ∅117
∅∅AD  ∅118
∅∅19  ∅119
∅∅8∅  ∅11A
```

FIG. 9. MESSAGE IN RESPONSE TO "B"

(d) Typing C for copy indicates that the content of the PROM is to be read and then stored in the microprocessor memory. The start and finish addresses of the PROM memory range and the start address of the microprocessor memory for storing the 8 bit data words is provided by the user in response to the message (Fig. 10). See Section 5.4.

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY C
PROM STARTS ∅∅∅∅ END ∅∅∅6, COPY FILE STARTS ∅5∅∅ END
∅5∅6
```

FIG. 10. MESSAGE IN RESPONSE TO "C"

5.2 Error Check

With "P" and "B" response the software automatically rereads each data byte word from the source file and compares it with that word that was previously stored in the PROM. Should the bit combination of the two words not be identical then an error is recorded.

The actual data word read from the PROM is displayed alongside the PROM and source file corresponding addresses, from which the data word comparison was made, as shown in Fig. 11.

```
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS ØlØØ END Ø134
PROM STARTS ØØØØ
BYTE; L FOR LOW, H FOR HIGH L
DATA ADDRESS
PROM PROM DATA
ØØØØ  ØØØØ  Ø13Ø
ØØØØ  ØØØ1  Ø131
ØØØØ  ØØØ2  Ø132
ØØØØ  ØØØ3  Ø133
ØØØØ  ØØØ4  Ø134
ERRORS ØØØ5
```

FIG. 11. MESSAGE CONTAINING ERROR LIST

The error tabulation concludes with the total number of byte errors recorded.

5.3 PROM Memory-List

Following the error check, if in "B" operation, or immediately after the message block in "L" operation, is displayed the PROM memory content in sequential address order (Fig. 8).

5.4 PROM Memory-Copy

In "C" operation the contents of the PROM are copied into the random access memory of the microprocessor. No direct listing is provided (Fig. 10) other than the end address of the copy file which is automatically appended to the "C" message block.

Normally the PROM package would then be removed from the zero force insertion socket of the PROM PROGRAMMER and replaced by an erased PROM. Following a "B" or "P" operation the cleared PROM contains a duplicate copy of the original PROM content.

Should a listing be desired then the "L" operation could be used or alternatively the executive read only memory (ROM) of the microprocessor used to list the contents of the specified memory addresses. In the latter case an advantage may be that the listing is more useful in an assembly code than in hexidecimal.

5.5 Program Cycle

During a write operation the PROM address and data byte words are latched and the control word bits changed during a program cycle to switch the various lines described in Section 2.2. The program

cycle, as specified by the PROM manufacturer, should be repeated until the data byte, being written into the specified PROM address reads true and then repeated five times that number of cycles. Thus if the PROM reads true after two program cycles then a total of twelve program cycles are called for before advancing to store the next data byte.

In practice however, the PROM data was found to consistently read true after only one program cycle. Therefore to simplify the operation and to avoid repeatedly switching between the read and write modes, each data byte is written into the same PROM address 10 times. When all memory addresses specified by the user have been accessed and programmed, the PROM content over the specified memory range is checked for errors, as described in Section 5.2.

This approach also overcomes the potential "no stop" situation should a fault occur that prevents the data from reading true and allows an accurate time estimate for writing into a PROM.

Based on a 2.8 millisec. pulse for the PROG line and a 20% duty cycle results in a write rate of about 7 data bytes/second or about 75 seconds to fully program 512 memory locations of a MM5204Q.

5.6 Flow Diagram

The controlling software requires less than 500 RAM locations and could easily be modified for ROM operation in conjunction with a small scratch pad of RAM. At present the allocated memory range is 020 to 01FF which precludes a source file, which is intended to be written into a PROM, from overlapping this address range.

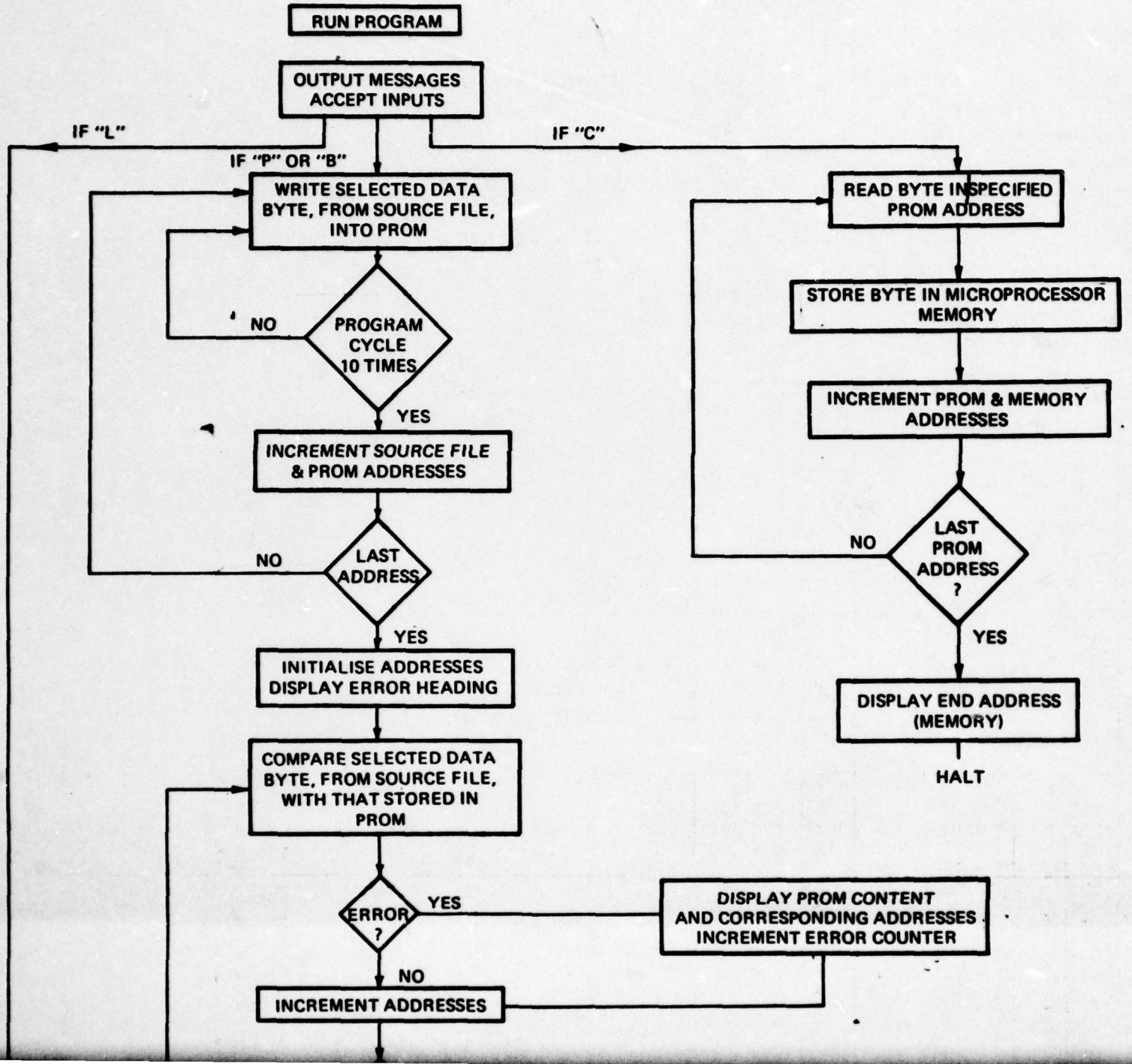
A simplified flow diagram for all user options is shown in Fig. 12.

5.7 Binary File Loader

The binary file which is to be temporarily stored in RAM before being written into PROM may be entered manually from a keyboard. However, the file will normally be dumped from the DEC-10 system having first been produced as an OBJECT file by a PACEX cross assembler from a SOURCE file.

Such a dump requires a loader program at the microprocessor to accept and store the bytes as these are received via conventional computer lines from the DEC-10 system.

An off-set loader program has been provided for this purpose and occupies the memory block between 04FD and 0609.


RUN PROGRAM
OUTPUT MESSAGES ACCEPT INPUTS
IF "L"
IF "P" OR "B"
IF "C"
WRITE SELECTED DATA BYTE, FROM SOURCE FILE, INTO PROM
NO
PROGRAM CYCLE 10 TIMES
YES
INCREMENT SOURCE FILE & PROM ADDRESSES
NO
LAST ADDRESS
YES
INITIALISE ADDRESSES DISPLAY ERROR HEADING
COMPARE SELECTED DATA BYTE, FROM SOURCE FILE, WITH THAT STORED IN PROM
ERROR ?
YES
DISPLAY PROM CONTENT AND CORRESPONDING ADDRESSES INCREMENT ERROR COUNTER
NO
INCREMENT ADDRESSES
READ BYTE IN SPECIFIED PROM ADDRESS
STORE BYTE IN MICROPROCESSOR MEMORY
INCREMENT PROM & MEMORY ADDRESSES
NO
LAST PROM ADDRESS ?
YES
DISPLAY END ADDRESS (MEMORY)
HALT

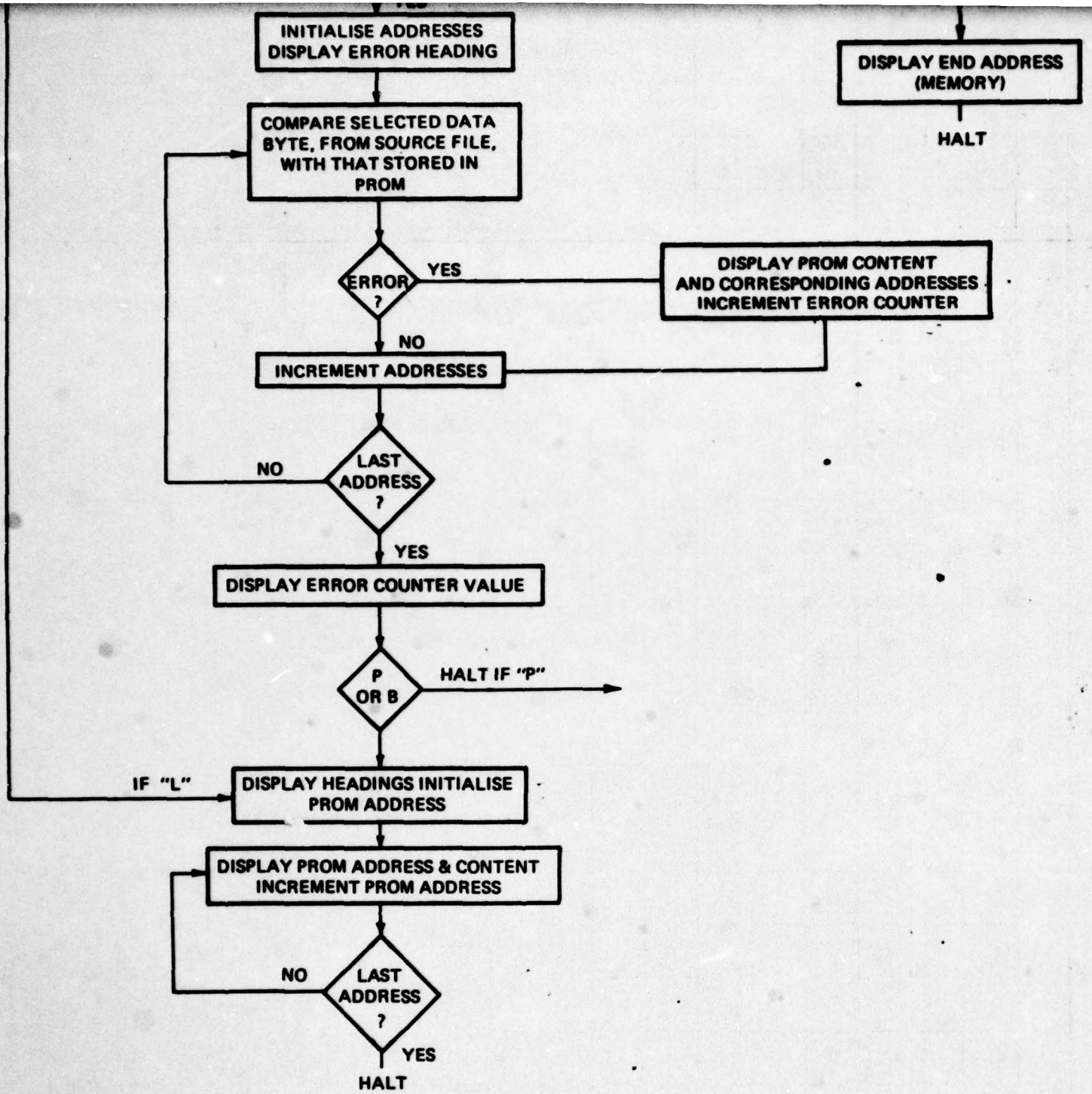


FIG. 12 FLOW DIAGRAM OF CONTROLLING SOFTWARE

If no off-set is required the loader starting address is 0500. The binary file is then stored in the specific memory addresses required for the program to run. However, such a choice of memory storage is not always practical since the binary file, which is the version that will be written into PROM, may require a memory block which is not duplicated by RAM of the PROM PROGRAMMER. Also, memory areas used by the prom programmer and loader programs are not available for storage of files which are to be written into PROM.

If an off-set is required the loader starting address is 0503 and a memory off-set value is deposited into 04FD. This enables the binary file to be stored in any available RAM block.

The off-set loader is not a relocatable loader thus the file cannot normally be run while resiging in the off-set memory locations. This is unimportant for the purpose of writing a previously proven file onto a PROM.

The use of the off-set loader is shown in Figs. 13 and 14.

```
PACE 2
>LD L
TI = LOADER
LO = Ø4FD
HI = Ø6Ø9
ST = Ø5ØØ

>RN Ø5Ø3
DEPOSIT LOAD OFFSET IN ADDRESS Ø4FD
HLT ØØ5ØA

>ST Ø4FD, Ø48ØØ

RN Ø5Ø3
READY
ENTER ADDRESS = F825
LO ADDRESS = 48ØØ + F8ØØ
HI ADDRESS = 48ØØ + ØØØØ
```

FIG. 13. OFF-SET LOADER RESPONSE.

In Fig. 13 details are shown where the off-set loader has been entered into the microprocessor memory from a paper tape reader. The title (TI) is LOADER with a high (HI) memory address of 0609 and a Low (LO) memory address of 04FD. For no off-set the program starts (ST) at 0500.

For the example given below an off-set value of 04800 has been set (ST) into address 04FD and the program rerun (RN) starting at 0503.

Example

Assume that the binary file as produced by the PACEX cross assembler requires a memory block 0F800 to 0FC00, which is the address range needed for the PROM version to run, and that microprocessor RAM exists starting at 04000. This is illustrated in Fig. 14.

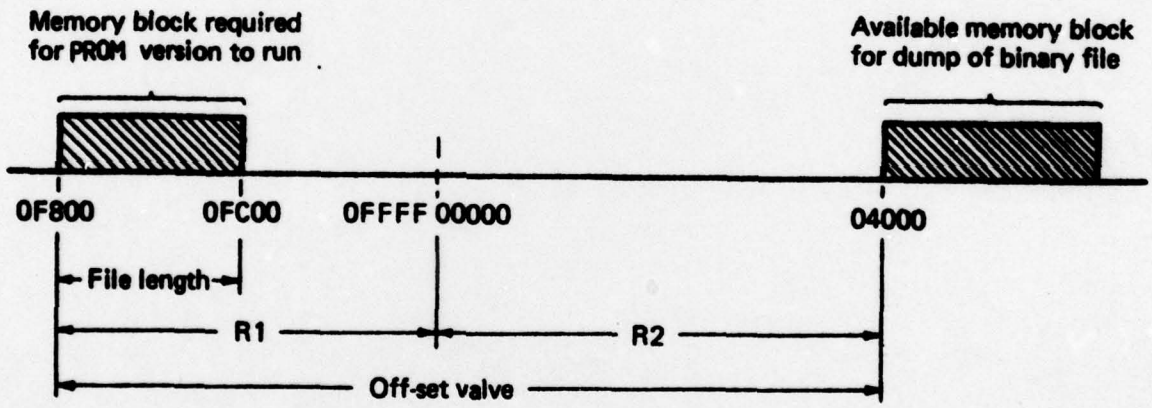


FIG. 14. MEMORY BLOCKS SHOWN FOR EXAMPLE

```
TI = PROM
CKS Ø174,12  I
REL BIN
LO = ØØ
HI = Ø1FF
ST = ØØ

>RN Ø16B
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS 4ØØØ END 41FF
PROM STARTS ØØØØ
BYTE; L FOR LOW, H FOR HIGH L
DATA ADDRESS
PROM PROM DATA
ERRORS ØØØØ
HLT ØØØCE

>

PACE 2

>RN Ø16B
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS 4ØØØ END 41FF
PROM STARTS ØØØØ
BYTE; L FOR LOW, H FOR HIGH H
DATA ADDRESS
PROM PROM DATA
ERRORS ØØØØ
HLT ØØØCE

>

PACE 2

>RN Ø16B
ENTER
    P FOR PROG, L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS 42ØØ END 43FF
PROM STARTS ØØØØ
BYTE; L FOR LOW, H FOR HIGH L
DATA ADDRESS
PROM PROM DATA
ERRORS ØØØØ
HLT ØØØCE
```

```
>

PACE 2

>RN ø16B
ENTER
    P FOR PROG., L FOR LIST, B FOR BOTH, C FOR COPY P
FILE STARTS 42øø END 43FF
PROM STARTS øøøø
BYTE; L FOR LOW, H FOR HIGH L
DATA ADDRESS
PROM PROM DATA
ERRORS øøøø
HLT øøøCE
```

FIG. 15. CONTROL PROGRAM RESPONSE FOR GIVEN EXAMPLE.

Two calculations are required;

(a) The length of the file to check that sufficient RAM is available to handle a single dump.

(b) The off-set value needed to dump the file into the RAM.

Calculations may be done directly, using the hexadecimal values, or hexadecimal to decimal conversion Tables used.

```
FILE LENGTH = 0FC00 - F800 = 0400 (hexadecimal)
     or       64512 - 63480 = 1024 (decimal)

OFF-SET VALUE = R1 + R2

                00000 - 0F800 + 04000 = 04800 (hex.)
     or         øFFFF + 1 - 0F800 + 04000
                65535 + 1 - 63488 + 16384 = 18432 (decimal).
```

The control program applicable to the example is shown in Fig. 15.

6. OPERATING INSTRUCTIONS

(a) Store binary file, which is to be written into PROM, in a selected memory block (exclude 020-01FF). See Section 6 if loader is to be used.

(b) Load control program "PROM" from paper tape or from cassette recorder.

If a PROM is to be copied, allocate a memory address block for this purpose.

(c) Insert a PROM package in the zero insertion force socket.

(d) Run control software starting at 016B and enter from keyboard information in response to messages.

(e) For a write operation press, and hold pressed, the SUPPLY switch just prior to entering H or L in response to BYTE message. Release switch only at completion of the write sequence, as signalled by the error message, to avoid errors.

This ensures that the -50 volt supply is only available to the PROM socket during the duration of a write operation.

DOCUMENT CONTROL DATA SHEET

Security classification of this page: UNCLASSIFIED

1. DOCUMENT NUMBERS
a. AR Number: AR-001-602
b. Document Series and Number: Aerodynamics Technical Memorandum 313
c. Report Number: ARL-AERO-TECH-MEMO-313

2. SECURITY CLASSIFICATION
a. Complete document: UNCLASSIFIED
b. Title in isolation: UNCLASSIFIED
c. Summary in isolation: UNCLASSIFIED

3. TITLE:

A MICROPROCESSOR CONTROLLED PROM PROGRAMMER

4. PERSONAL AUTHOR:

C.W. SUTTON

5. DOCUMENT DATE: February, 1979

6. TYPE OF REPORT AND PERIOD COVERED: Tech. Memo.

7. CORPORATE AUTHOR:

8. REFERENCE NUMBERS
a. Task: DST 76/103
b. Sponsoring Agency:

9. COST CODE: 577720

10. IMPRINT:

11. COMPUTER PROGRAM(S) (Title(s) and Language(s):

12. RELEASE LIMITATIONS (of the document):

Approved for Public Release.

12-0. OVERSEAS:	NO		P.R.	1	A		B		C		D		E		

13. ANNOUNCEMENT LIMITATIONS (of the information on this page):

No Limitation.

14. DESCRIPTORS:
Computer Storage Devices. Microprocessors
Computer Programs. PROM
Programmable Read. Only Memory (PROM)

15. COSATI CODES: 0902

16. ABSTRACT:

This paper describes a microprocessor controlled PROM programmer with user options to program, list and copy the memory content of MM5204Q devices.

DISTRIBUTION

	COPY NO.
AUSTRALIA	
Department of Defence	
Central Office	
Chief Defence Scientist	1
Deputy Chief Defence Scientist	2
Superintendent, Science and Technology Programs	3
Australian Defence Scientific and Technical Representative (UK)	4
Counsellor, Defence Science	5
Joint Intelligence Organisation	6
Defence Library	7
Assistant Secretary, D.I.S.B.	8-23
Aeronautical Research Laboratories	
Chief Superintendent	24
Superintendent - Aerodynamics Division	25
Divisional file - Aerodynamics	26
Author - C.W. Sutton	27
Library	28
Inst. Group File	29-30
Inst. Annexe	31-32
Materials Research Laboratories	
Library	33
Defence Research Centre Salisbury	
Library	34
SPARES	35-44